Electronics 1: Chapter 2 figs

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Note that the source code for the figs can be seen by clicking the pic. You will need to use your Browser's BACK button to return to this page.

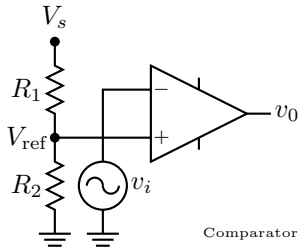

Figure 1: The Comparator

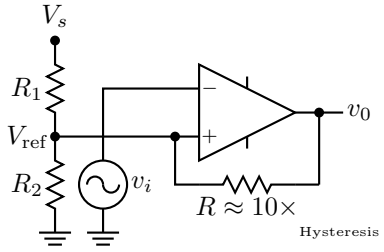

Figure 2: Positive Feedback causes state-dependant thresholds

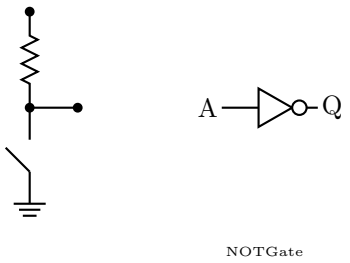

Figure 3: An Inverter

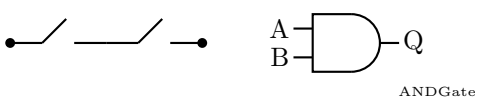

Figure 4: The AND Gate

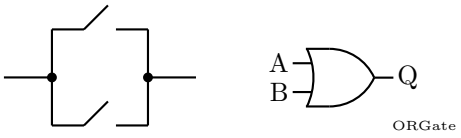

Figure 5: The OR Gate

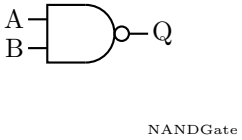

Figure 6: The NAND Gate

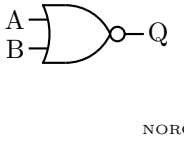

Figure 7: The NOR Gate.

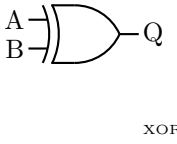

Figure 8: The XOR Gate

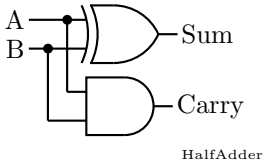

Figure 9: A Half Adder

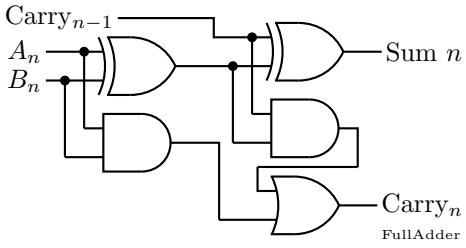

Figure 10: A Full Adder

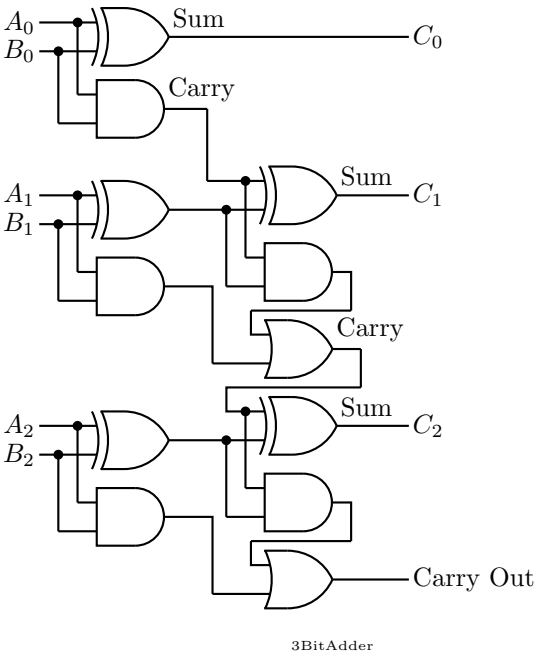

Figure 11: 3 Bit Adder!

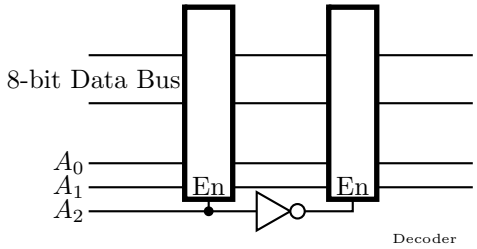

Figure 12: Simplest decoder to select between two 4-byte memories

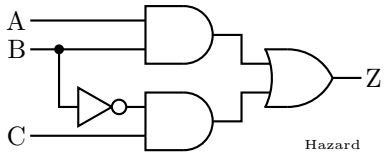

Figure 13: Timing Hazard.

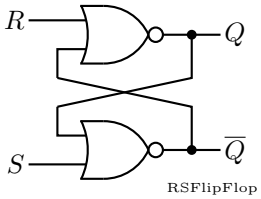

Figure 14: The RS (Reset-Set) Flip Flop

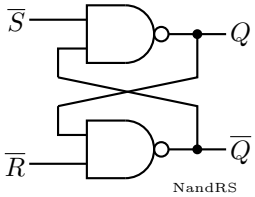

Figure 15: A Nand-based RS Flip Flop.

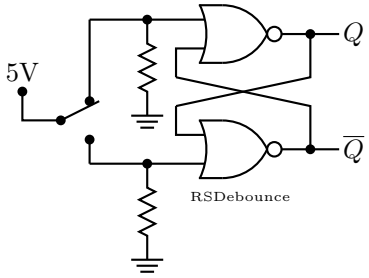

Figure 16: An RS Flip Flop used in debouncing

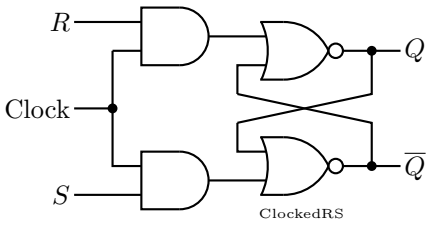

Figure 17: A Clocked RS Flip Flop

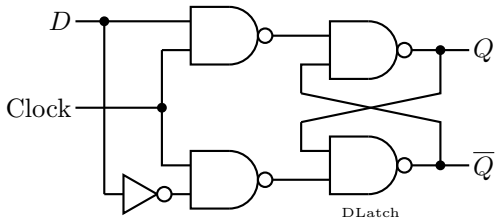

Figure 18: NAND gate D Latch

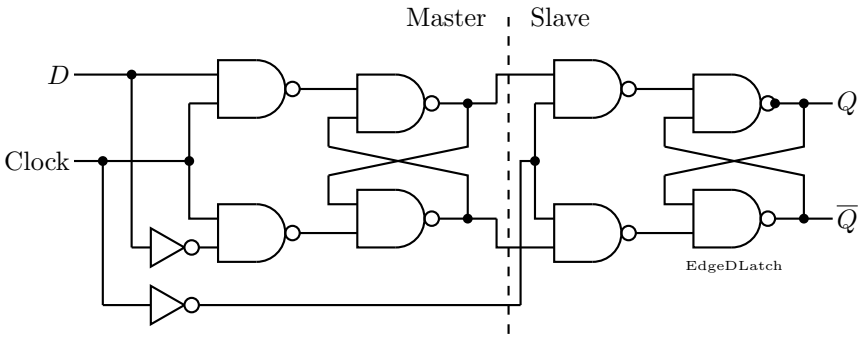

Figure 19: A neg Edge Triggered Master-Slave Flip Flop